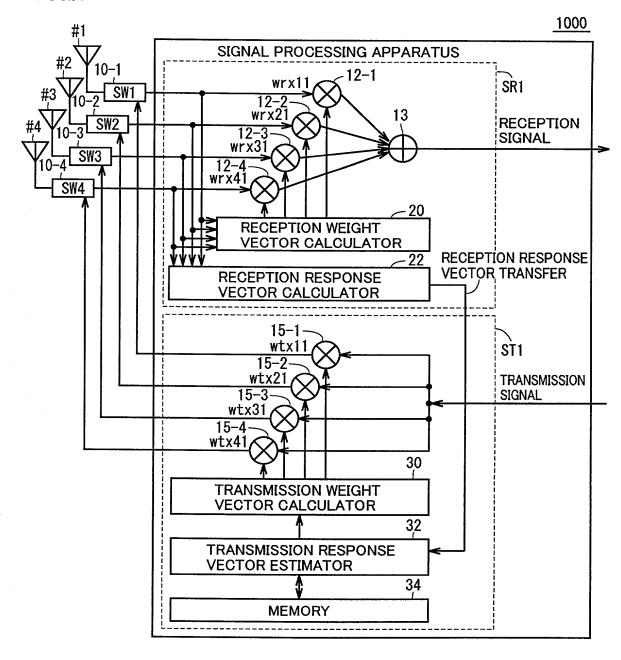
FIG.1



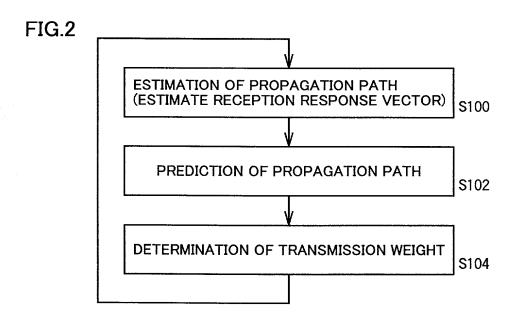


FIG.3

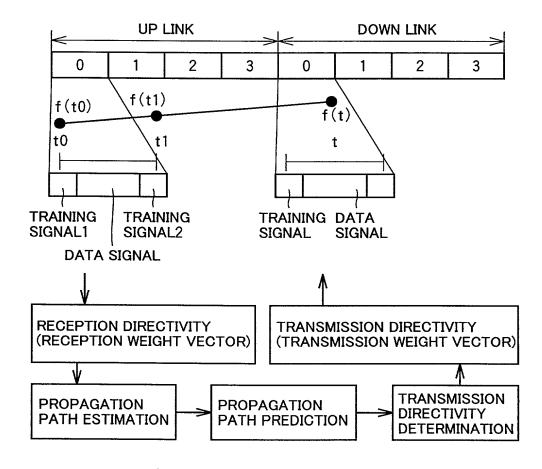


FIG. 4A

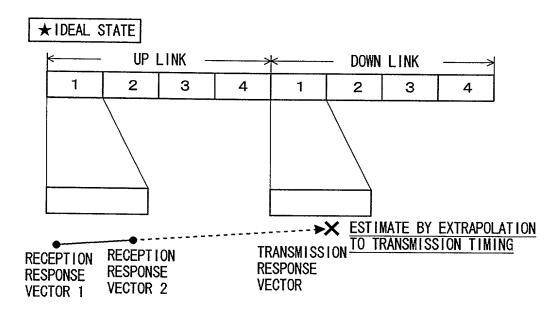
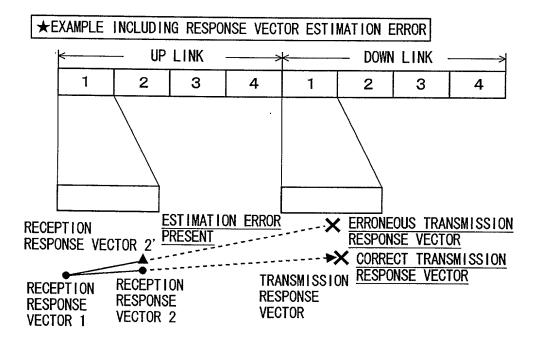
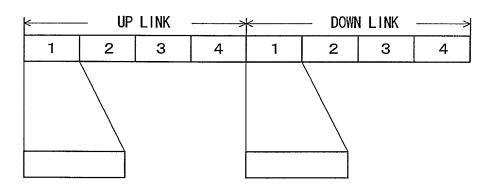
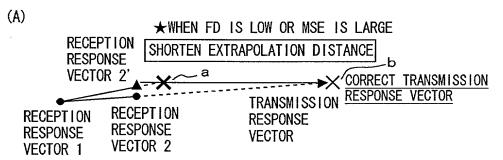


FIG. 4B



F I G. 5





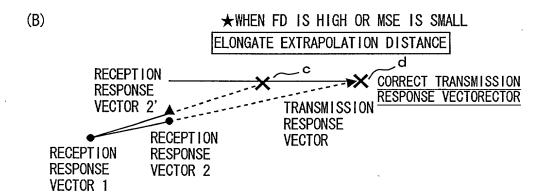
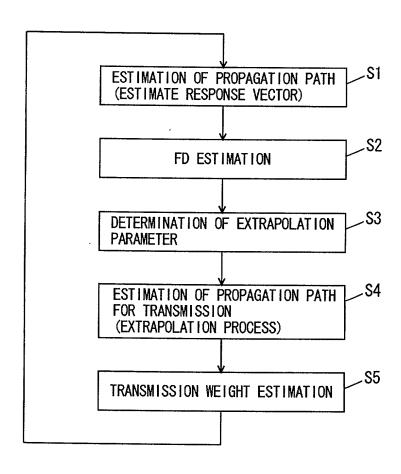
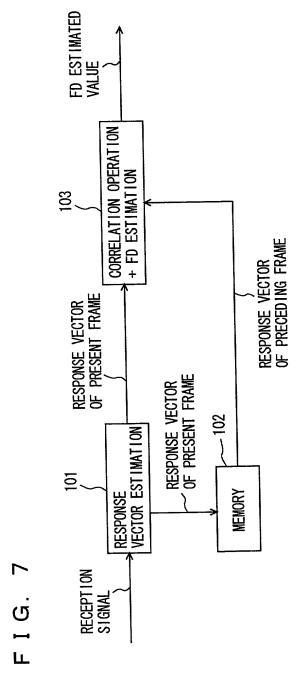
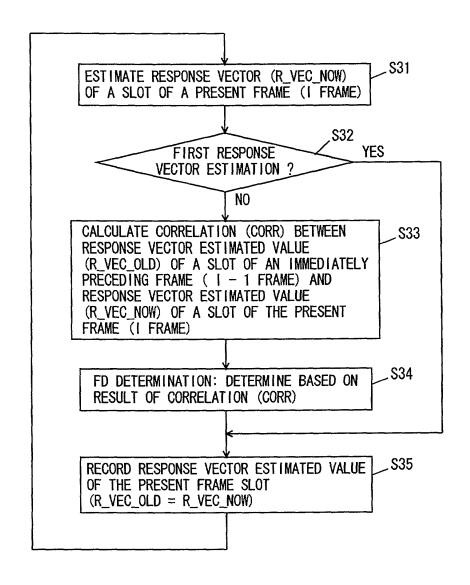


FIG. 6





## F I G. 8



F I G. 9

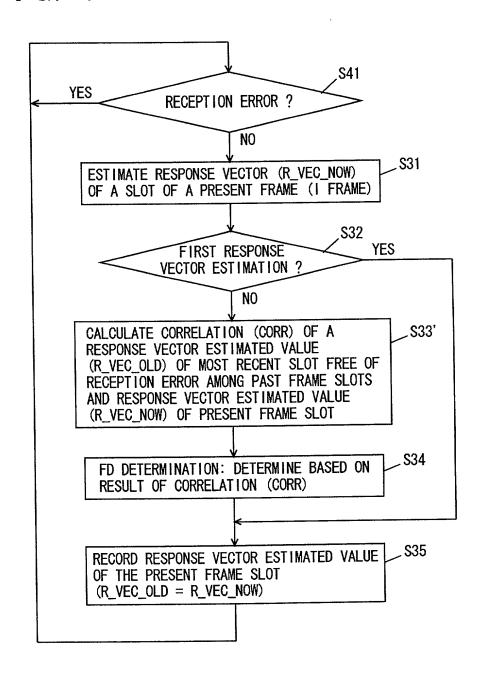


FIG. 10

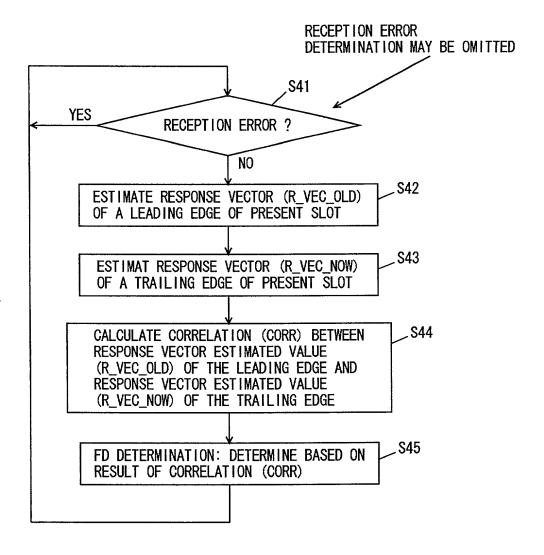


FIG. 11

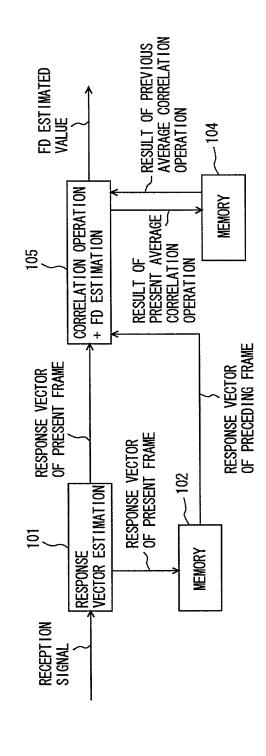


FIG. 12

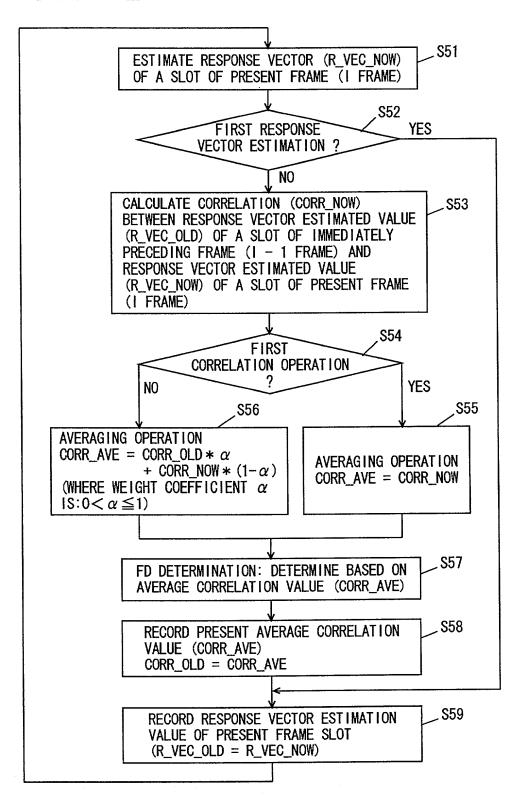
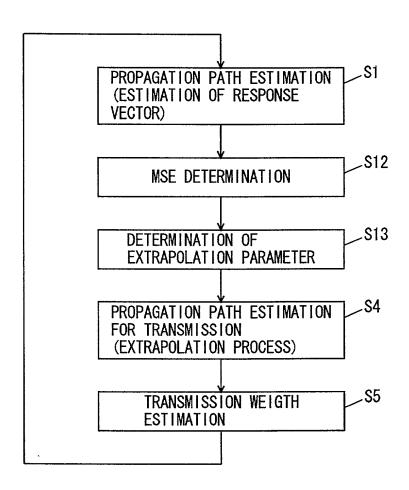


FIG. 13



## FIG. 14

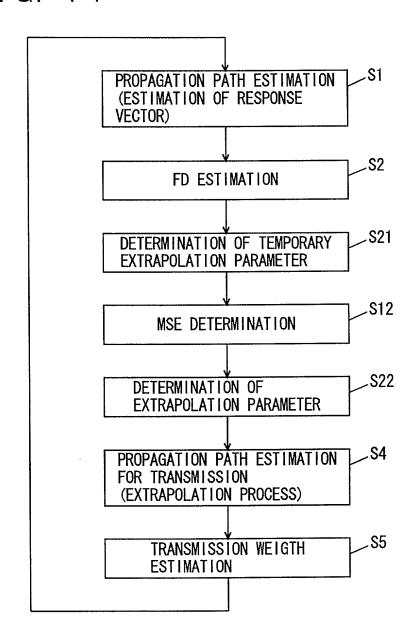


FIG.15 PRIOR ART

(C)PDMA PATH DIVISION MULTIPLE ACCESS	f1 CHANNEL1 CHANNEL2   f1 CHANNEL3 CHANNEL4				14   CHANNEL23   CHANNEL24
(B) TDMA TIME DIVISION MULTIPLE ACCESS	f1   CHANNEL1   CHANNEL2	f2   CHANNEL3   CHANNEL4	f3   CHANNEL5   CHANNEL6	f4   CHANNEL7   CHANNEL8	
(A) FDMA FREQUENCY DIVISION MULTIPLE ACCESS	FREQUENCY  A f1 CHANNEL1	f2 CHANNEL2	f3 CHANNEL3	f4 CHANNEL4	

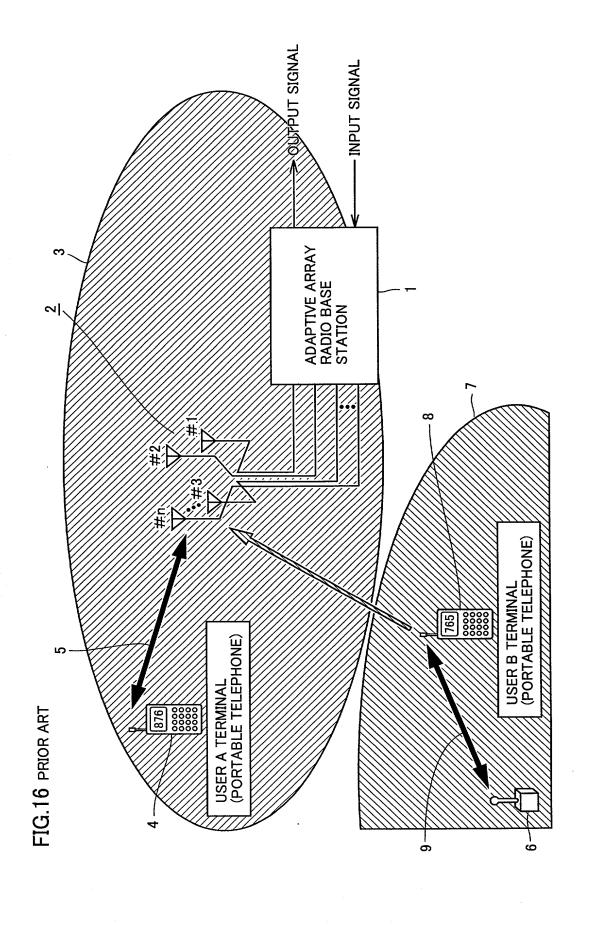


FIG.17 PRIOR ART

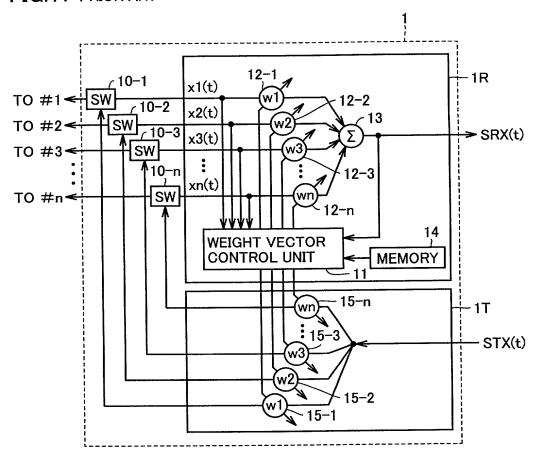


FIG.18 PRIOR ART

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